PATENT
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	)	Docket: NVIDP011/P000094
	)	
Lindholm et al.	)	Examiner: HAVAN, T.
	)	Group Art Unit: 2671
Serial No.: Unknown	)	
	)	Date: October 26, 2001
Filed: October 26, 2001	)	
	)	
For: LIGHTING SYSTEM AND	)	
METHOD FOR A GRAPHICS	)	
PROCESSOR (AS AMENDED)	)	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on October 26, 2001.

Signed: Erica L. Mann
Erica L. Mann

PRELIMINARY AMENDMENT

Commissioner for Patents
and Trademarks
Washington, DC 20231

Dear Sir:

Before the substantive examination of the above application, please enter the following amendments:

IN THE TITLE

Please delete the TITLE OF THE INVENTION, and insert therefore:

LIGHTING SYSTEM AND METHOD FOR A GRAPHICS PROCESSOR

IN THE SPECIFICATION

Please delete lines 7-24 on page 1, and insert therefor: (See Appendix A for redlined copy)

The present application is a continuation of an application filed 12/06/99 under serial number 09/454,524. The present application is further related to applications entitled "Method, Apparatus and Article of Manufacture for Area Rasterization using Sense Points" which was filed on December 06, 1999 under serial number 09/455,305, and attorney docket number NVIDP005, "Method, Apparatus and Article of Manufacture for Boustrophedonic Rasterization" which was filed on December 06, 1999 under serial number 09/454,505, and attorney docket number NVIDP006, "Method, Apparatus and Article of Manufacture for Clip-less Rasterization using Line Equation-based Traversal" which was filed on December 06, 1999 under serial number 09/455,728, and attorney docket number NVIDP007, "Method, Apparatus and Article of Manufacture for Transform, Lighting and Rasterization on a Single Semiconductor Platform" which was filed on December 06, 1999 under serial number 09/454,516, and attorney docket number NVIDP008, "Method, Apparatus and Article of Manufacture for a Vertex Attribute Buffer in a Graphics Processor" which was filed on December 06, 1999 under serial number 09/454,525, and attorney docket number NVIDP009, "Method, Apparatus and Article of Manufacture for a Transform Module in a Graphics Processor" which was filed on December 06, 1999 under serial number 09/456,102, and attorney docket number NVIDP010, and "Method, Apparatus and Article of Manufacture for a Sequencer in a Transform/Lighting Module Capable of Processing Multiple Independent Execution Threads" which was filed on December 06, 1999 under serial number 09/456,104, and attorney docket number NVIDP012 which were filed concurrently herewith, and which are all incorporated herein by reference in their entirety.

On page 5, please delete lines 7-15, and insert therefor: (See Appendix A for redlined copy)

Figure **1** illustrates the prior art;

Figure **1A** is a flow diagram illustrating the various components of one embodiment of the present invention implemented on a single semiconductor platform;

On page 11, please delete the first paragraph and insert therefore: (See Appendix A for redlined copy)

Figure **1** illustrates the prior art. Figures **1A-32C** show a graphics pipeline system of the present invention.

On page 11, please delete the second paragraph and insert therefore: (See Appendix A for redlined copy)

Figure **1A** is a flow diagram illustrating the various components of one embodiment of the present invention. As shown, the present invention is divided into four main modules including a vertex attribute buffer (VAB) **50**, a transform module **52**, a lighting module **54**, and a rasterization module **56** with a set-up module **57**. In one embodiment, each of the foregoing modules is situated on a single semiconductor platform in a manner that will be described hereinafter in greater detail. In the present description, the single semiconductor platform may refer to a sole unitary semiconductor-based integrated circuit or chip.

IN THE CLAIMS

Please delete claims 1-23, and add claims 24-41 as follows:

24. A lighting system for graphics processing, comprising:

(a) at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom;

(b) a multiplication logic unit coupled to the at least one input buffer;

(c) an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit;

(d) a register unit coupled to the arithmetic logic unit; and

(e) a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit.

25. The system as recited in claim 24, wherein the multiplication logic unit has a feedback loop coupled to an input thereof.

26. The system as recited in claim 24, wherein the lighting logic unit is coupled to the multiplication logic unit via a conversion module adapted for converting scalar vertex data to vector vertex data.

27. The system as recited in claim 24, wherein the arithmetic logic unit and the multiplication logic unit include multiplexers.

28. The system as recited in claim 24, wherein the multiplication logic unit includes three multipliers coupled in parallel.

29. The system as recited in claim 24, wherein the arithmetic logic unit includes three adders coupled in series and parallel.

30. A lighting system for graphics processing, comprising:

(a) at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom;

(b) a multiplication logic unit coupled to the at least one input buffer;

(c) an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit;

(d) a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit; and

(e) memory coupled to the multiplication logic unit and the arithmetic logic unit.

31. The system as recited in claim 30, wherein the memory includes a plurality of constants for processing the vertex data.

32. The system as recited in claim 30, wherein the memory has a read terminal coupled to the multiplication logic unit.

33. The system as recited in claim 30, wherein the memory has a write terminal coupled to the arithmetic logic unit.

34. A lighting system for graphics processing, comprising:

(a) a multiplication logic unit;

(b) an arithmetic logic unit coupled to the multiplication logic unit;

(c) a register unit coupled to the arithmetic logic unit;

(d) a lighting logic unit coupled to the arithmetic logic unit and the multiplication logic unit; and

(e) memory coupled to the multiplication logic unit and the arithmetic logic unit.

35. A lighting system for graphics processing, comprising:

(a) at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom; and

(b) a lighting logic unit adapted for receiving the vertex data;

(c) wherein the lighting logic unit is capable of setting a flag upon the vertex data satisfying predetermined criteria.

36. A method for flagging in a graphics processing module, comprising:

(a) processing vertex data in a graphics processing module;

(b) outputting the processed vertex data; and

(c) setting at least one flag upon the vertex data satisfying predetermined criteria.

37. The method as recited in claim 36, wherein the graphics processing module is a lighting module.

38. The method as recited in claim 37, wherein a lighting logic unit of the lighting module sets the flag.

39. The method as recited in claim 36, and further comprising clamping a value of an attribute of the vertex data based on the setting of the flag.

40. A computer program product for flagging in a graphics processing module, comprising:

(a) computer code for processing vertex data in a graphics processing module;

(b) computer code for outputting the processed vertex data; and

(c) computer code for setting a flag upon the vertex data satisfying predetermined criteria.

41. A graphics processing system, comprising:

(a) logic for processing vertex data in a graphics processing module;

(b) logic for outputting the processed vertex data; and

(c) logic for setting a flag upon the vertex data satisfying predetermined criteria.

REMARKS

Additional claims have been added which reflect what was set forth in the originally filed application. Further, the specification has been amended to conform with the figures, as originally filed. No new matter has been added.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100.

Respectfully submitted,

Kevin J. Zilka
Registration No. 41,429

P.O. Box 721120
San Jose, CA 95172-1120
Telephone: (408) 505-5100